Exhibit A

BEST AVAILABLE COPY

Planar gap prefill process for read he...

Disclosure SJO8-1999-0008

Created By: Douglas Werner **Created On:** 01/18/99 10:34:33 AM
Last Modified By: Alma Silva **Last Modified On:** 01/18/99 02:46:41 PM

*** IBM Confidential ***

Required fields are marked with the asterisk (*) and must be filled in to complete the form.

Summary

Status	Under Evaluation
Processing Location	SJO
Functional Area	Wafer/Read Head - Scranton
Attorney/Patent Professional	Palk Saber/San Jose/IBM
IDT Team	Kathy A Diaz/San Jose/IBM; Joseph Smyth/San Jose/IBM; Prakash Kasiraj/Almaden/IBM; Palk Saber/San Jose/IBM
Submitted Date	01/18/99 02:19:36 PM
Owning Division	SSD
PVT Score	To calculate a PVT score, use the 'Calculate PVT' button.

Inventors with Lotus Notes ID's

Inventors: Douglas Werner/San Jose/IBM

Inventor Name > denotes primary contact	Inventor Serial	Div/Dept	Manager Serial	Manager Name
Werner, Doug (Douglas)	767170	35/E6CA	43150Z	Clarke, Thomas G

Inventors without Lotus Notes ID's

IDT Selection

Main Idea

Title of disclosure (in English)

Planar gap prefill process for read heads

Idea of disclosure

1. Describe your invention, stating the problem solved (if appropriate), and indicating the advantages of using the invention.

The invention creates a planar surface with multiple insulator (first read gap) thicknesses. The thick gap areas provide better electrical insulation (read head - first shield), while the thin gap areas are required in the read sensor region to permit large bit densities. Such tailoring of insulator thicknesses is prior art, but it produces a physical step (nonplanarity) in the first gap, over which the read head sensor is deposited and photolithographically defined (Figure 1). This step can cause two problems in the subsequent photolithography: (1)reflective notching caused by light scattering from the step, and (2)nonuniform photoresist coverage over the steps which compromises control of critical printed dimensions (CD's) due to the "swing curve" effect (where CD's vary with photoresist thickness due to constructive & destructive interference of reflected light within the photoresist film). The invention solves both problems by creating a planar surface on which the read head sensor is deposited and photolithographically defined (Figure 2).

The figures are in the following attachment:

PlanarPrefill.P

BEST AVAILABLE COPY

2. How does the invention solve the problem or achieve an advantage,(a description of "the invention", including figures inline as appropriate)?
In prior art read head processing, the first read (sensor) gap is deposited over a prior patterned (extra-insulation) gap, leaving behind the problematic step near the sensor. These processes are typically done after planarizing the first shield (S1) and preceding steps w/ chemical-mechanical polishing (CMP). In the invention, the extra-insulation gap process creates a nearly planar surface by patterning with an established bilayer photoresist stencil process, then removing a some S1 material by ion milling to a predetermined depth, then refilling with gap insulator material of a thickness slightly less than the milled depth (Figure 3), then lifting off the stencil over the sensor region (the areas where the read head leads will be placed enjoy the benefit of the extra insulating gap material). The CMP step is deferred until after the patterning just described, and serves to remove any residual nonplanarity around the sensor region of the read head. Then, as in the prior art, the (sensor) gap and sensor materials are deposited and patterned to define the read head.

3. If the same advantage or problem has been identified by others (inside/outside IBM), how have those others solved it and does your solution differ and why is it better?

CD variation caused by device topography is a problem commonly encountered in microelectronics fabrication, and it is typically controlled by either (1)addition of antireflective layers, or (2)planarization. In the existing IBM read head build process, the planarization approach is preferred since it involves only an additional ion milling step, while anti reflective layers are only partially effective and introduce complications associated with their removal. While planarization has been used to address the present problem, I am not aware of prior art which uses the same process sequence to arrive at the structure described.

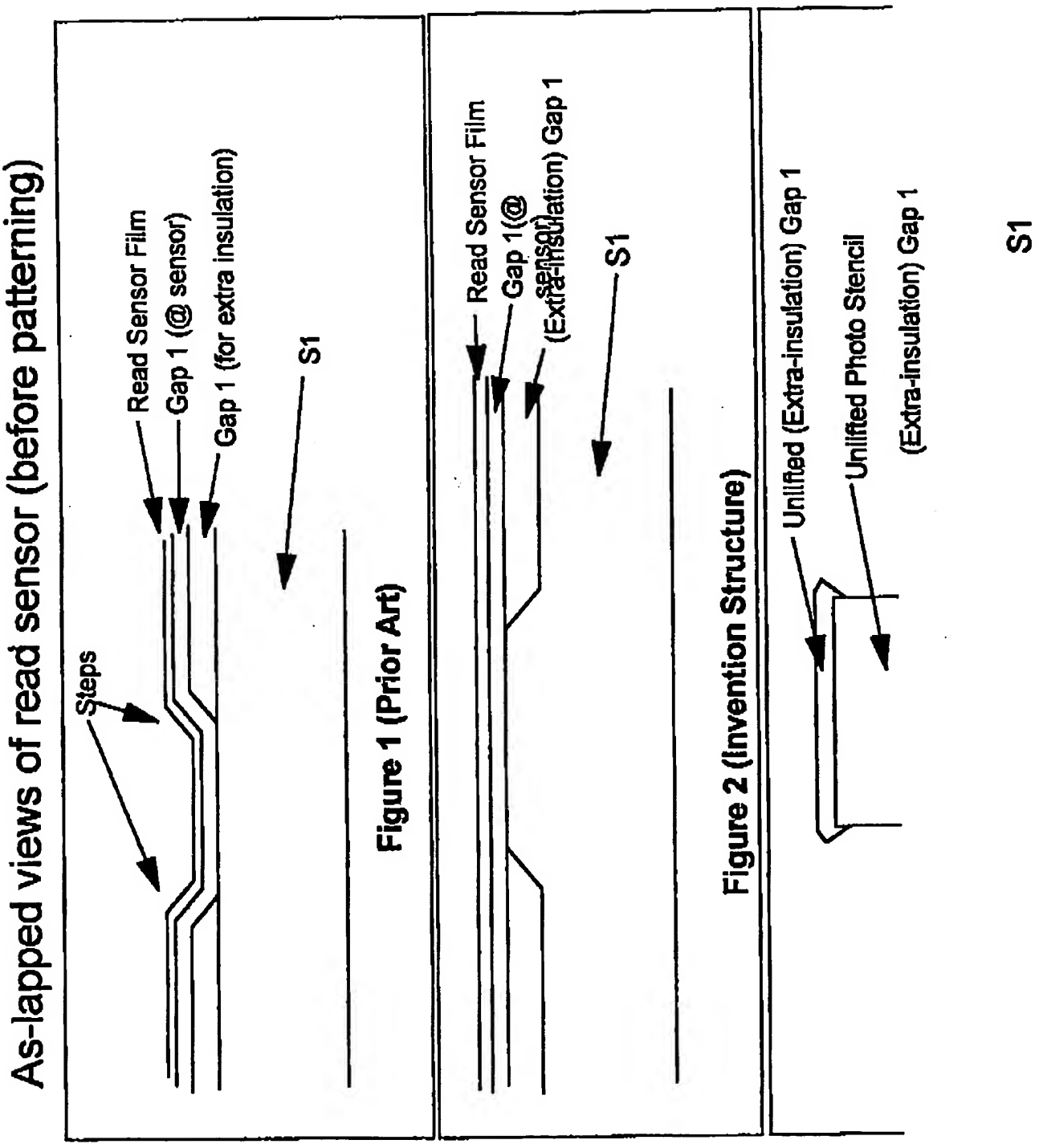
4. If the invention is implemented in a product or prototype, include technical details, purpose, disclosure details to others and the date of that implementation.
TBD. No implementation yet.

***Critical Questions (Questions 1 - 7 must be answered)**

*Question 1
On what date was the invention workable? - private - Please format the date as MM/DD/YY
(Workable means i.e. when you know that your design will solve the problem)

*Question 2
Is there any planned or actual publication or disclosure of your invention to anyone outside IBM? ○ Yes ● No
If yes, Enter the name of each publication or patent and the date published below.
Publication/Patent
Date Published or Issued
Are you aware of any publications, products or patents that relate to this invention? ○ Yes ● No
If yes, Enter the name of each publication or patent and the date published below.
Publication/Patent
Date Published or Issued

*Question 3
Has the subject matter of the invention of a product incorporating the invention been sold, used internally in manufacturing, announced for sale, or included in a proposal? ○ Yes ● No
If sale, use in manufacturing, product announcement or proposal planned? ○ Yes ● No


As-lapped views of read sensor (before patterning)
Steps
Read Sensor Film
Gap 1 (@ sensor)
Gap 1 (for extra insulation)
S1
Figure 1 (Prior Art)
Read Sensor Film
Gap 1 (@ sensor)
(Extra-insulation) Gap 1
S1
Figure 2 (Invention Structure)
Unlifted (Extra-insulation) Gap 1
Unlifted Photo Stencil
(Extra-insulation) Gap 1
S1